AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:

a direct memory access (DMA) controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller terminates a DMA transfer and clears a current transfer counter before a terminal count is reached upon receiving an early termination request signal from the I/O device.

2. (Previously Presented) The system of claim 1 wherein the DMA controller re-executes a DMA transfer with the I/O device upon receiving a retransmit request signal from the I/O device.

Claims 3-5. (Cancelled)

6. (Original) The system of claim 1 further comprising:

a system interconnect coupled to the I/O device and the DMA controller;

a central processing unit (CPU) coupled to the system interconnect; and

a memory device coupled to the system interconnect.

Claims 7-11. (Cancelled)

12. (Currently Amended) A system comprising:

a direct memory access (DMA) controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller re-executes a DMA transfer from the beginning with the I/O device upon receiving a retransmit request signal from the I/O device.

13. (Currently Amended) A method comprising:

transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the

first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

re-transferring the data from the beginning between the first device and the second device.

14. (Original) The method of claim 13 further comprising reloading configuration registers within the DMA controller prior to transmitting the acknowledge signal to the first device.

15. (Previously Presented) A method comprising:

transferring data between a first device and a second device under control of a direct memory access (DMA) controller;

receiving a request signal at the DMA controller from the first device indicating a request by the first device to terminate the transfer of data between the first device and the second device;

erasing appropriate DMA controller information in order to restart the transfer of data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

16. (Original) The method of claim 13 [[further comprising]] wherein the erasing comprises, clearing a counter within the DMA controller prior to transmitting the acknowledge signal to the first device.

Claims 17-20. (Cancelled)

21. (Previously Presented) The method of claim 15 further comprising:

receiving a second request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

re-transferring the data between the first device and the second device according to the first set of commands.

22. (Previously Presented) The method of claim 15 further comprising:

receiving a second request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

23. (Original) The method of claim 22 further comprising:

reducing a transfer count within the descriptor table after terminating the transfer; and

retrieving a second set of commands from the descriptor table.

24. (Previously Presented) The system of claim 1 wherein the DMA controller comprises a first channel coupled to the I/O device to facilitate the transfer of data.

25. (Previously Presented) The system of claim 24 wherein the DMA controller further comprises a register, coupled to the channel, to store configuration data.

26. (Previously Presented) The system of claim 25 wherein the DMA controller further comprises error checking logic.

27. (Previously Presented) The system of claim 24 wherein the channel comprises control logic to control the transfer process within the first channel.

28. (Previously Presented) The system of claim 24 wherein the channel further comprises descriptor logic to control the transfer of data in a descriptor mode.

29. (Previously Presented) The system of claim 12 wherein the DMA controller comprises a first channel coupled to the I/O device to facilitate data transfers.

30. (Previously Presented) The system of claim 29 wherein the DMA controller further comprises a register, coupled to the channel, to store configuration data.

31. (Previously Presented) The system of claim 30 wherein the DMA controller further comprises error checking logic.

32. (Previously Presented) The system of claim 29 wherein the channel comprises control logic to control the transfer of data.